CLAIMS

What is claimed is:

1. A data processing apparatus, comprising:

(a) a memory;

(b) a direct memory access controller operatively coupled to said memory;

(c) a cyclic redundancy check circuit operatively coupled to said direct memory access controller;

(d) said direct memory access controller configured to transfer data from said memory to said cyclic redundancy check circuit; and

(e) said cyclic redundancy check circuit configured to calculate at least one check value for said data.

2. The apparatus of claim 2, further comprising stored programming configured to seed said cyclic redundancy check circuit with a selected initial value.

3. The apparatus of claim 2, wherein said stored programming is further configured to set up said direct memory access controller with a source address for a data stream, a destination address for said data stream, and a size for said data stream.

4. The apparatus of claim 3, wherein said stored programming is further configured to initiate transfer of said data stream by said direct memory access controller from said memory to said cyclic redundancy check circuit.

5. The apparatus of claim 4, wherein said stored programming is further configured to read a calculated cyclic redundancy check value from said cyclic redundancy check circuit and store said calculated cyclic redundancy check value in said memory.

6. The apparatus of claim 1, further comprising a display controller operatively coupled to said direct memory access controller, said direct memory access controller configured to transfer a display data stream from said memory to said display controller.

7. The apparatus of claim 6 further comprising stored programming configured to set up said display controller with a display address for said display data stream.

8. The apparatus of claim 7 further comprising stored programming configured to set up said direct memory access controller with a source address for said display data stream, a destination address for said display data stream, and a size for said display data stream.

9. The apparatus of claim 8, further comprising stored programming configured to initiate transfer of said display data stream by said direct memory access controller to said display controller.

10. The data processing apparatus of claim 1, further comprising:

(a) programming stored in said memory capable of seeding said cyclic redundancy check circuit with a selected initial value;

(b) programming stored in said memory capable of setting up said direct memory access controller with a source address for a data stream, a destination address for said data stream, and a size for said data stream; and

(c) programming stored in said memory capable of initiating transfer of said data stream by said direct memory access controller to said cyclic redundancy check circuit.

11. The data processing apparatus of claim 6, further comprising:

(a) programming stored in said memory capable of setting up said display controller with a display address for a display data stream;

(b) programming stored in said memory capable of setting up said direct memory access controller with a source address for said display data stream, a display address for said display data stream, and a size for said display data stream; and

(c) programming stored in said memory capable of initiating transfer of said data stream by said direct memory access controller to said display controller.

12. A method for processing data, comprising:

(a) transferring a data stream from a memory to a cyclic redundancy check circuit using a direct memory access controller; and

(b) calculating a cyclic redundancy check value for said data stream by said cyclic redundancy check circuit.

13. The method of claim 12, wherein said transferring comprises seeding said cyclic redundancy check circuit with a selected initial value.

14. The method of claim 13, wherein said transferring said data stream to said cyclic redundancy check circuit further comprises setting up said direct memory access controller with a source address for said data stream, a destination address for said data stream, and a size for said data stream.

15. The method of claim 14, wherein said transferring said data stream to said cyclic redundancy check circuit further comprises initiating transfer of said data stream by said direct memory access controller to said cyclic redundancy check circuit.

16. The method of claim 15, wherein said transferring said data stream to said cyclic redundancy check circuit further comprises transferring each byte in said data stream to said cyclic redundancy check circuit by said direct memory access controller.

17. The method of claim 12, further comprising reading a calculated cyclic redundancy check value from said cyclic redundancy check circuit and storing said calculated cyclic redundancy check value in said memory.

18. The method of claim 12, further comprising transferring a display data stream from said memory to a display controller using said direct memory access controller.

19. The method of claim 18, wherein said transferring said display data stream to said display controller comprises setting up said display controller with a display address for said display data stream.

20. The method of claim 19, wherein said transferring said display data stream to said display controller further comprises setting up said direct memory access controller with a source address for said display data stream, a destination address for said display data stream, and a size for said display data stream.

21. The method of claim 20, wherein said transferring said display data stream to said display controller further comprises initiating transfer of said display data stream by said direct memory access controller to said display controller.

22. A data processing apparatus, comprising:

(a) direct memory access controller means for transferring a data stream from a memory to a cyclic redundancy check circuit; and

(b) means for calculating a cyclic redundancy check value for said data stream by said cyclic redundancy check circuit.

23. The apparatus of claim 22, further comprising program means for seeding said cyclic redundancy check circuit with a selected initial value.

24. The apparatus of claim 23, further comprising program means for setting up said direct memory access controller means with a source address for said data stream, a destination address for said data stream, and a size for said data stream.

25. The apparatus of claim 24, further comprising program means for initiating transfer of said data stream by said direct memory access controller means to said cyclic redundancy check circuit.

26. The apparatus of claim 22, further comprising means for reading a calculated cyclic redundancy check value from said cyclic redundancy check circuit and storing said calculated cyclic redundancy check value in said memory.